WHAT IS CLAIMED IS:

1. A memory management unit configured to receive a virtual address and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

2. The memory management unit as recited in Claim 1, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits comprises a predetermined value.

3. The memory management unit as recited in Claim 2, wherein the predetermined value is zero.

4. The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an arithmetic logic unit.

5. The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an incrementor.

6. The memory management unit as recited in Claim 1, wherein the virtual address comprises a data address.

7. The memory management unit as recited in Claim 1, wherein the virtual address comprises an instruction address.

8. The memory management unit as recited in Claim 1, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

9. The memory management unit as recited in Claim 1, wherein only virtual address-to-physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

10. The memory management unit as recited in Claim 1, wherein the storage is configured to store one or more most recently generated virtual address-to-physical address translations.

11. A system comprising:

an antenna;

a memory; and

a processor coupled to the antenna and memory, the processor comprising:

an address generation unit; and

a memory management unit configured to receive a virtual address from the address generation unit and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

12. The system as recited in Claim 11, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

13. The system as recited in Claim 11, wherein the address generation unit comprises an arithmetic logic unit.

14. The system as recited in Claim 11, wherein the address generation unit comprises an incrementor.

15. The system as recited in Claim 11, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

16. The system as recited in Claim 11, wherein only virtual address-to-physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

17. A method comprising:

receiving a virtual address;

determining if the virtual address has a translation to a physical address in a storage;

if not, generating a modified virtual address from the virtual address; and

translating the modified virtual address into a physical address.

18. The method as recited in Claim 17, wherein generating the modified virtual address comprises replacing one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

19. The method as recited in Claim 17, wherein translating the modified virtual address comprises performing a page table walk.

20. The method as recited in Claim 17, further comprising invalidating all translations in the storage if a process identifier changes.

21. The method as recited in Claim 17, further comprising invalidating only translations in the storage having a virtual address portion that has one or more bits equal to a predetermined value.

22. The method as recited in Claim 17, further comprising placing any generated translations into the storage.

23. The method as recited in Claim 17, wherein the virtual address is a data address.

24. The method as recited in Claim 17, wherein the virtual address is an instruction address.